MOS-GATED POWER DEVICE HAVING EXTENDED TRENCH AND DOPING ZONE AND PROCESS FOR FORMING SAME

FIELD OF THE INVENTION

The present invention relates to semiconductor devices and, more particularly, to a trench MOS-gated power device having an extended doped zone separated from a drain zone by an extended trench.

BACKGROUND OF THE INVENTION

An MOS transistor having a trench gate structure offers important advantages over a planar transistor for high current, low voltage switching applications. The DMOS trench gate typically includes a trench extending from the source to the drain and having sidewalls and a floor that are each lined with a layer of thermally grown silicon dioxide. The lined trench is filled with doped polysilicon. The structure of the trench gate allows less constricted current flow and, consequently, provides lower values of specific on-resistance. Furthermore, the trench gate makes possible a decreased cell pitch in an MOS channel extending along the vertical sidewalls of the trench from the bottom of the source across the body of the transistor to the drain below. Channel density is thereby increased, which reduces the contribution of the channel to on-resistance. The structure and performance of trench DMOS transistors are discussed in Bulucea and Rossen, "Trench DMOS Transistor Technology for High-Current (100 A Range) Switching," in *Solid-State Electronics,* 1991, Vol. 34, No. 5, pp 493–507, the disclosure of which is incorporated herein by reference. In addition to their utility in DMOS devices, trench gates are also advantageously employed in insulated gate bipolar transistors (IGBTs), MOS-controlled thyristors (MCTs), and other MOS-gated devices.

FIG. **1** schematically depicts the cross-section of a trench-gated N-type MOSFET device **100** of the prior art formed on an upper layer **101***a* of an N+ substrate **101**. Device **100** includes a trench **102** whose sidewalls **104** and floor **103** are lined with a gate dielectric such as silicon dioxide. Trench **102** is filled with a conductive material **105** such as doped polysilicon, which serves as an electrode for gate region **106**.

Upper layer **101***a* of substrate **101** further includes P-well regions **107** overlying an N-drain zone **108**. Disposed within P-well regions **107** at an upper surface **109** of upper layer **101***a* are heavily doped P+ body regions **110** and heavily doped N+ source regions **111**. An interlevel dielectric layer **112** is formed over gate region **106** and source regions **111**. Contact openings **113** enable metal layer **114** to contact body regions **110** and source regions **111**. The rear side **115** of N+ substrate **101** serves as a drain.

Although FIG. **1** shows only one MOSFET, a typical device currently employed in the industry consists of an array of them arranged in various cellular or stripe layouts. As a result of recent semiconductor manufacturing improvements enabling increased densities of trench gated devices, the major loss in a device when in a conduction mode occurs in its lower zone, i.e., increased drain resistivity. Because the level of drain doping is typically determined by the required voltage blocking capability, increased drain doping for reducing resistivity is not an option. Thus, there is a need for reducing the resistivity of the drain region in a semiconductor device without also reducing its blocking capability. The present invention meets this need.

SUMMARY OF THE INVENTION

The present invention is directed to a trench MOS-gated device that comprises a doped monocrystalline semiconductor substrate that includes an upper layer and is of a first conduction type. An extended trench in the substrate has a bottom portion filled with a dielectric material that forms a thick layer in the bottom of the trench. The upper portion of the trench is lined with a dielectric material and substantially filled with a conductive material, the filled upper portion of the trench forming a gate region.

An extended doped zone of a second opposite conduction type extends from an upper surface into the upper layer of the substrate on one side of the trench, and a doped well region of the second conduction type overlying a drain zone of the first conduction type is disposed in the upper layer on the opposite side of the trench. The drain zone is substantially insulated from the extended zone by the thick dielectric layer in the bottom portion of the trench.

A heavily doped source region of the first conduction type and a heavily doped body region of the second conduction type is disposed in the well region at the upper surface of the upper layer. An interlevel dielectric layer is disposed on the upper surface overlying the gate and source regions, and a metal layer disposed on the upper surface of the upper layer and the interlevel dielectric layer is in electrical contact with the source and body regions and the extended zone.

The present invention is further directed to a process for constructing a trench MOS-gated device that comprises forming an extended trench in an upper layer of a doped monocrystalline semiconductor substrate of a first conduction type, and substantially filling the trench with a dielectric material. A dopant of a second opposite conduction type is implanted and diffused into the upper layer on one side of the extended trench, thereby forming a doped extended zone extending into the upper layer from its upper surface.

A selected portion of the dielectric material is removed from an upper portion of the trench, leaving a thick dielectric layer in its bottom portion. Sidewalls comprising dielectric material are formed in the upper portion of the trench, which is then substantially filled with a conductive material, thereby forming a gate region in the upper portion of the trench.

A doped well region of the second conduction type is formed in the upper layer of the substrate on the side of the trench opposite the doped extended zone. A heavily doped source region of the first conduction type and a heavily doped body region of the second conduction type are formed in the well region at the upper surface of the upper layer. An interlevel dielectric layer is deposited on the upper surface overlying the gate and source regions, and a metal layer is formed over the upper surface and the interlevel dielectric layer, the metal layer being in electrical contact with the source and body regions and the extended zone.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** schematically depicts a cross-section of a trench MOS-gated device **100** of the prior art.

FIG. **2** is a schematic cross-sectional representation of a trench MOS-gated device **200** of the present invention.

FIGS. **2**A–D schematically depict a process for forming device **200** of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In FIG. **2** is schematically depicted the cross-section of an MOS-gated power device **200** of the present invention. In an upper layer **201***a* of a substrate **201** is constructed an extended trench **202** that is partially filled with dielectric